MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 3, 2018/2019

ECE4116 – DIGITAL COMPUTER DESIGN

(All sections / Groups)

01 JUNE 2019
09:00 a.m – 11:00 a.m
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 4 pages including cover page with 4 Questions only.
2. Attempt **ALL** questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please print all your answers in the Answer Booklet provided.

Question 1

(a) The sum-of-product minterms Boolean function of a logic circuit is given as:

$F(a, b, c, d) = \sum m(3, 5, 6, 7, 8, 12, 13, 14)$

(i) Draw the truth table for this logic circuit. [4 marks]

(ii) Implement the logic circuit by using a 4-to-1-line multiplexer and appropriate logic gates. Connect input a and b to the selection line of the multiplexer. [8 marks]

(b) The Finite State Machine (FSM) for a sequential circuit is shown in Figure Q1(b), which has two inputs, X and Y, and an output Z.

(i) Draw the Algorithmic State Machine (ASM) chart for the FSM in Figure Q1(b). [5 marks]

(ii) Design the sequential circuit using the one flip-flop per state technique. [8 marks]

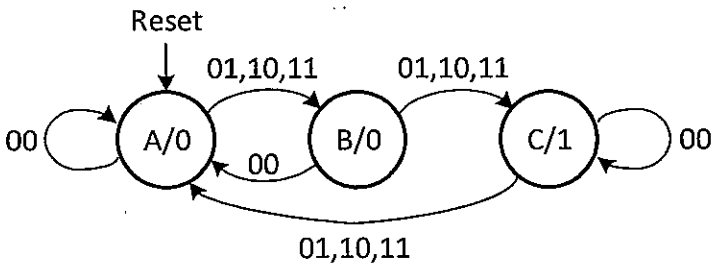

Figure Q1(b)

Question 2

(a) A digital system has TWO (2) registers, RA and RB, and control signals $C1$, $C2$ and $C3$. The control signals control the following register transfers:

$C1: RA \leftarrow RB$

$C2: RA \leftarrow \overline{RB}$

$C3: RA \leftarrow RA + RB$; (logical OR)

All the control signals are mutually-exclusive. When none are '1', no transfers occur. Design the logic circuit to implement the register transfers and draw the one-bit slice logic diagram. [10 marks]

(b) List (3) THREE basic arithmetic microoperations and provide an example using register transfer statement for each of them. [3 marks]

(c) A 16K×8 RAM is to be constructed from multiple 4K×8 RAM chips.

(i) Determine the number of address lines available on each 4K×8 RAM chip.

[2 marks]

(ii) Compute the number of address lines needed for the 16K×8 RAM

[2 marks]

(iii) Draw the block diagram of the 16K×8 RAM using 4K×8 RAM chips and a decoder. Show all address lines, data lines and control inputs.

[8 marks]

Continued...

Question 3

(a) Inputs X and Y of each full adder in an arithmetic circuit have digital logic specified by the following Boolean functions:

$X_i = A_i$

$Y_i = \bar{B}_i S + B_i \bar{C}_{in}$

where S is a selection variable, C_{in} is the input carry, A_i and B_i are input data for the current stage

(i) Draw the logic diagram of a typical single-bit stage of the 4-bit circuit, using a full adder and a multiplexer. [6 marks]

(ii) Determine the arithmetic operation performed for $S = 1$ and $C_{in} = 1$.

[2 marks]

(b) Find the output Y of the 4-bit barrel shifter in Figure Q3(b) for each of the following bit patterns applied to control signal S_1, S_0, and data signal D_3, D_2, D_1, D_0.

(i) 010101 [2 marks]

(ii) 101001 [2 marks]

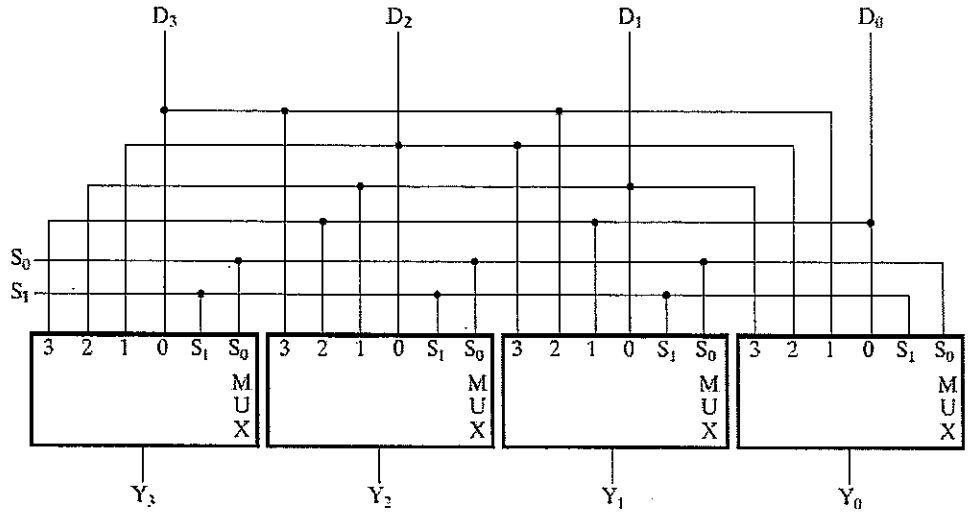

Figure Q3(b)

(c) A hypothetical computer has ONE (1) general-purpose register, $R1$. The instruction set includes instructions MOV (move), ADD (add), SUB (subtract), MUL (multiply) and DIV (divide). All instructions specify TWO (2) memory addresses, where the first one is an operand (if applicable) and the destination. Given the arithmetic expression:

$$A = (P - Q) + R/S$$

where A, P, Q, R, S denote memory addresses,

(i) Write the instructions to evaluate the arithmetic expressions and store the result in memory location A. [5 marks]

(ii) State the number of memory accesses required. Subsequently, state how the number of memory accesses can be reduced.

[3 marks]

Continued...

(d) A simple computer uses 16-bit wide data and hardwired control. Figure Q3(d) shows the format of its immediate-mode instruction.

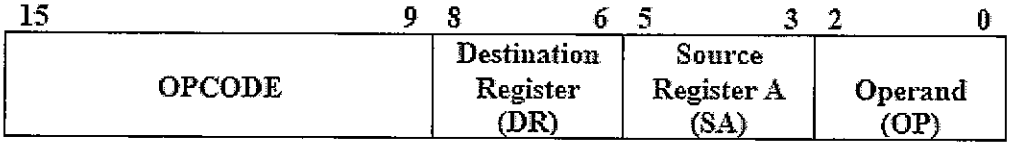

Figure Q3(d)

The 3-bit operand (OP) in the instruction must be extended to 16 bits in the control unit. State the TWO (2) operations that can be used to achieve this and briefly describe the difference between them.

[5 marks]

Question 4

(a) The sequence of four LDI instructions given in Table Q4(a) is fetched and executed by a RISC CPU with four pipeline stages.

Table Q4(a)

LDI	R1,2
LDI	R3,4
LDI	R5,6
LDI	R7,8

Manually simulate the execution by giving, for each clock cycle, the value in pipeline registers *PC*, *IR*, *Data A*, *Data B*, *Data F*, and the relevant register for each clock cycle. Assume that the first given instruction is at memory address *N*. Assume that all registers initially contains -1. [12 marks]

(b) A hypothetical RISC machine employs a typical 4-stage pipeline. The following sequence of instructions is executed.

```
MOVA    R1, R5
SLT     R2, R4, R1
BNZ     R2, 25
MOVA    R5, R8
```

(i) Draw the pipeline execution diagram to show the execution of the instructions. Subsequently, identify all hazards and specify what type they are. [7 marks]

(ii) Describe the methods to resolve the hazards identified in part (i). [6 marks]

End of Paper